CLAIMS

What is claimed is:

1. A subthreshold current-efficient buffer comprising:
   first and second inverters connected in series;
   a memory cell;
   an NMOS transistor controlled by the memory cell and connected between the second inverter and ground.

2. The subthreshold current-efficient buffer of claim 1 further including a PMOS transistor controlled by a complemented output of the memory cell and connected between the first inverter and a power source.

3. The subthreshold current-efficient buffer of claim 1 where the first inverter comprises a PMOS transistor manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

4. A subthreshold current-efficient circuit comprising:
   first and second buffers, each buffer having two inverters connected in series;
   an NMOS transistor connected in series between ground and the second inverter of each buffer.

5. The subthreshold current-efficient circuit of claim 4 further comprising a memory cell controlling the NMOS transistor.

6. The subthreshold current-efficient circuit of claim 4 wherein the first and second buffers each comprise PMOS transistors manufactured to sit in a voltage well

biased with a higher voltage than that of a power supply.

7. The subthreshold current-efficient circuit of claim 6 wherein the PMOS transistors form part of the first inverter of each buffer.

8. In a field programmable device having logic blocks and a routing matrix, an improved subthreshold current-efficient circuit comprising:

at least one buffer for driving signals onto a signal line of the routing matrix;

an NMOS transistor connected between ground and the at least one buffer;

a memory cell connected to control the NMOS transistor and turn it off when the at least one buffer is unused.

9. The field programmable device of claim 8 further comprising a PMOS transistor connected between a power supply and the at least one buffer and controlled by the memory cell.

10. The field programmable device of claim 8 wherein the buffer comprises at least one PMOS transistor manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

11. In a field programmable device having CLEs and a routing matrix, an improved subthreshold current efficient circuit comprising:

a plurality of buffers for driving signals on signal lines of the routing matrix, the plurality of buffers being grouped in pairs wherein each buffer pair comprises an NMOS transistor connected between ground and the buffer pair;

a corresponding memory cell connected to control each NMOS transistor and turn it off when its associated buffer pair is unused.

12. The field programmable device of claim 11 further comprising a PMOS transistor connected between a power supply and each buffer, the corresponding memory cell connected to control each PMOS transistor and turn it off when its associated buffer pair is unused.

13. The field programmable device of claim 11 wherein the plurality of buffers comprise at least one PMOS transistor manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

14. A method of reducing subthreshold current in a field programmable device comprising the steps of:

providing virtual ground transistors on selected buffers within an FPD;

providing memory cells to control the state of the virtual ground transistors;

programming the memory cells to turn off the virtual ground transistors of the buffers that are not being used.

15. The method of claim 14 further comprising providing virtual power transistors on selected buffers within the FPD and controlling the state of the virtual power transistors by programming the memory cells to turn off the virtual power transistors of the buffers that are not being used.

16. The method of claim 14 further comprising providing selected buffers within the FPD which have PMOS transistors manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

17. The method of claim 14 further comprising providing virtual ground transistors to control logic gates used as the first stage of a buffer.